VIAVI Solutions

Data Sheet

VIAVI
Xgig Jammer for PCIe 5.0

for PCI Express® 5.0

Jamming (Error Injection) enables testing and evaluation of fault recovery operation

The VIAVI Jammer brings error injection (jamming) ability to the Xgig® PCI Express systems. A jammer is an essential tool for hardware controller state machine validation and protocol stack validation of system software. A jammer enables testing of boundary and stress conditions that are not common to normal system operation and would otherwise be difficult to check.

The PCIe 5.0 Jammer supports operation at all PCIe data rates of 2.5, 5.0, 8.0, 16 and 32GTps. All lane widths are also supported; 1, 2, 4, 8 and 16 lanes.

The Jammer function is normally combined with an Analyzer in an Analyzer-Jammer (AJ) configuration. To see input and output data on all lanes and both before and after jamming, a second Analyzer is used in the Analyzer-Jammer-Analyzer (AJA) configuration.

Interposers provide the connection between the Xgig PCIe 5.0 Analysis system chassis and the devices under test (DUTs) supporting the jammer function. VIAVI offers a variety of Interposers providing physical connections for popular system applications.

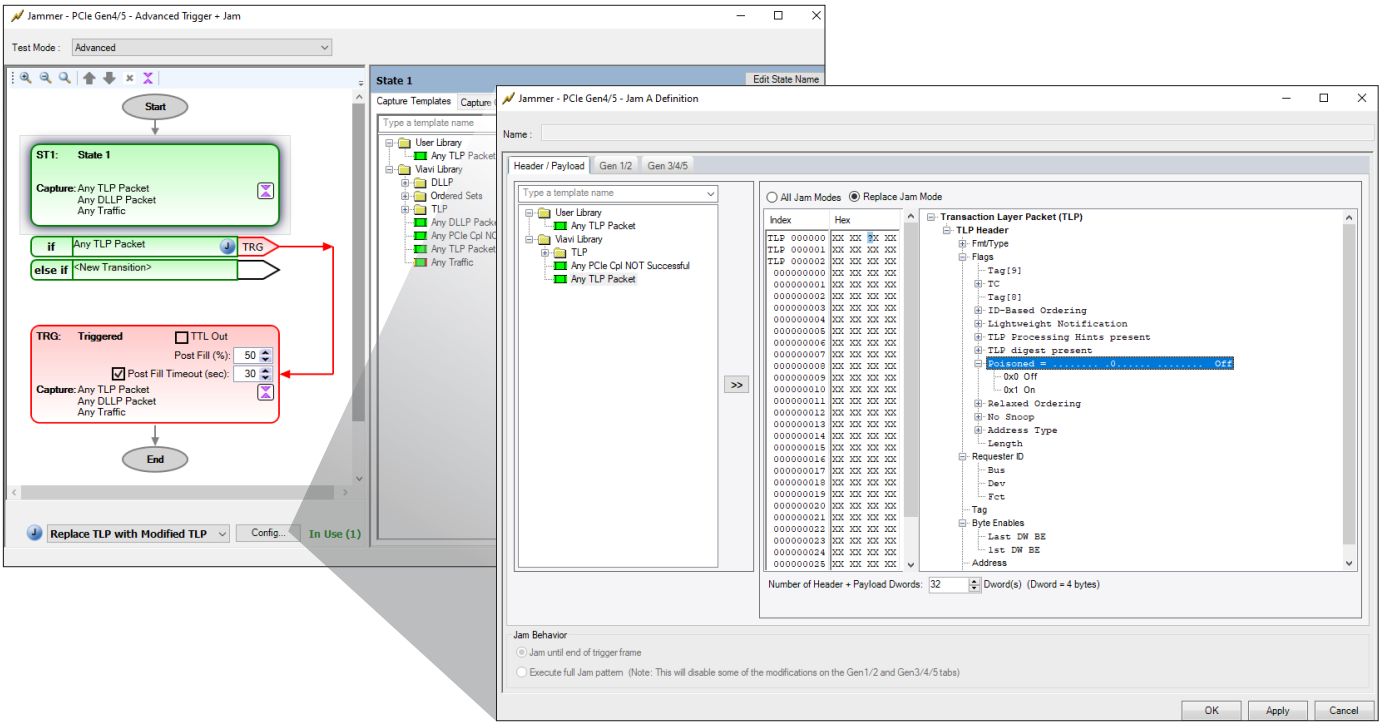
Custom Jammer test configurations can be defined, either new or edited from existing or library configurations. The Jammer Test Suite API allows complex test sequences to be specified.

When operating in Jammer mode, or Analyzer/Jammer mode, data flows through the Analyzer Chassis between DUT devices. Xgig analysis tools are installed and run on a local or remote Windows PC.

Features

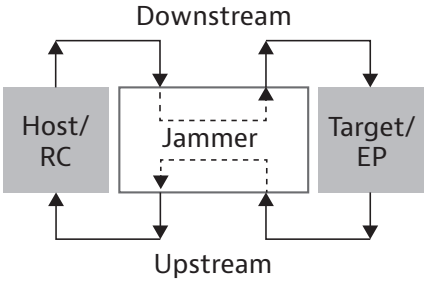
- Jammer runs on VIAVI 5P16 or 5P8 PCIe 5 analysis platform chassis
- Supports all PCIe data rates to 32GTps
- Supports link widths of 1, 2, 4, 8 and 16-lanes
- Operates in Jammer only, Analyzer-Jammer (AJ) and Analyzer-Jammer-Analyzer (AJA) configurations
- Supported by VIAVI PCIe Interposers
- Define Arm and Trigger conditions
- Repeat test suite sequences or TLP repetition
- Replace TLP packets. Change header or payload.
- Swap DLLP ACK to NACK. Replace CRC.
- Modify Ordered Sets
- Replace TLP or DLLP with idle
- Real-time ECRC and LCRC recalculation
- Trigger a jam from up-to 7-states, each with up to three conditions
- Offers complex logic for custom jam conditions
- Define custom test configurations; save and load
- Define custom test suites and execution sequence
- Template libraries available
- Scripting API allows complex test cases
- Graphical control interface provides easy visual presentation and setup of test procedures
- Supported by Xgig Analysis Software Tool suite for Windows

Xgig Jammer Graphical Configuration Interface



Applications

The picture at right is a conceptual diagram of Jammer operation. The Jammer fits into the PCIe data path separating the link into two segments. Either upstream, downstream or both can be jammed simultaneously with VIAVI tools.



An Xgig Chassis runs the Jammer function. Note that the interposer for physical interface is not diagrammed.

VIAVI offers Jammers which run on chassis platforms for PCIe 5.0 and PCIe 4.0. Jammer License for 16-lane, 8-lane or 4-lane operation are available to match your specific test requirements.

Ordering Information (for PCIe 5.0 Platforms)

Part Number	Description
Xgig5P-PCIe5-X16-JM	Xgig 16-lane Jammer License Key for PCIe 5.0
Xgig5P-PCIe5-X8-JM	Xgig 8-lane Jammer License Key for PCIe 5.0
Xgig5P-PCIe5-X4-JM	Xgig 4-lane Jammer License Key for PCIe 5.0

VIAVI Solutions

Contact Us **+1 844 GO VIAVI**
(+1 844 468 4284)

To reach the VIAVI office nearest you,
visit viavisolutions.com/contact

xgigjammer-ds-snt-nse-ae
30193049 900 0321